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UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5218561

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June 8, 1993

Fast calculation apparatus for carrying out a forward and an inverse transform

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INVENTOR: Iwadare, Masahiro - Tokyo, Japan (JP)

APPL-NO: 712888 (07)

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ASSIGNEE-PRE-ISSUE: July 12, 1991 - ASSIGNMENT OF ASSIGNORS INTEREST., NEC CORPORATION 7-1, SHIBA 5-CHOME, MINATO-KUTOKYO, (1), Reel and Frame Number: 005781/0055

ASSIGNEE-AT-ISSUE: NEC Corporation, Tokyo, Japan (JP), Foreign company or corporation (03)

ENGLISH-ABST:

In an apparatus for carrying out a linear transform calculation on a product signal produced by multiplying a predetermined transform window function and an apparatus input signal, an FFT part (23) carries out fast Fourier transform on a processed signal produced by processing the product signal in a first processing part (21). As a result, the FFT part produces an internal signal which is representative of a result of the fast Fourier transform. A second processing part (22) processes the internal signal into a transformed signal which represents a result of the linear transform calculation. The apparatus is applicable to either of forward and inverse transform units (11, 12).

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** SS 1: Results 1

Search statement 2

Query/Command : prt full nonstop legalall

1 / 1 PLUSPAT - Questel
PN - US5218561 A 19930608 [US5218561]
TI - (A) FAST CALCULATION APPARATUS FOR CARRYING OUT A FORWARD AND AN
INVERSE TRANSFORM
PA - (A) NIPPON ELECTRIC CO (JP)
PA0 - NEC Corporation, Tokyo [JP]
IN - (A) IWADARE MASAHIRO (JP)
AP - US71288891 19910612 [1991US-0712888]
PR - JP15166290 19900612 [1990JP-0151662]
IC - (A) G06F-007/38
ICAA- H04N-007/30 [2006-01 A F I R M JP]; G06F-017/14 [2006-01 A - I R M
EP]; G10L-011/00 [2006-01 A L I R M JP]; G10L-015/02 [2006-01 A L
I R M JP]; G10L-019/00 [2006-01 A L I R M JP]; H04N-001/41
[2006-01 A L I R M JP]
ICCA- H04N-007/30 [2006 C F I R M JP]; G06F-017/14 [2006 C - I R M EP];
G10L-011/00 [2006 C L I R M JP]; G10L-015/00 [2006 C L I R M JP];
G10L-019/00 [2006 C L I R M JP]; H04N-001/41 [2006 C L I R M JP]
EC - G06F-017/14F2
PCL - ORIGINAL (O) : 708400000
DT - Corresponding document
CT - H. Nussbaumer, "Fast Multidimensional Discrete Cosine Transforms",
IBM Technical Disclosure Bulletin, vol. 23, No. 5, Oct. 1980, pp.
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- Schiller, N., "Overlapping Block Transform Image Coding
Preserving Equal Number of Samples and Coefficients", SPIE vol.
1001 Visual Communications and Image Processing 1988, pp. 834-839.
STG - (A) United States patent
AB - In an apparatus for carrying out a linear transform calculation on
a product signal produced by multiplying a predetermined
transform window function and an apparatus input signal, an FFT
part (23) carries out fast Fourier transform on a processed signal
produced by processing the product signal in a first processing
part (21). As a result, the FFT part produces an internal signal
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A second processing part (22) processes the internal signal into
a transformed signal which represents a result of the linear
transform calculation. The apparatus is applicable to either of
forward and inverse transform units (11, 12).

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AP - US71288891 19910612 [1991US-0712888]
PUB - 19910612 US-API [POS; EXM]
FILING DETAILS
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19930608 US-A [POS; EXM]
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US5218561 A 19930608 [US5218561]
ACT - 19910712 US/AS02-A [NMC]
ASSIGNMENT OF ASSIGNOR'S INTEREST
OWNER: NEC CORPORATION 7-1, SHIBA 5-CHOME, MINATO-KU TOKY;
EFFECTIVE DATE: 19910628

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OWNER: IWADARE, MASAHIRO; EFFECTIVE DATE: 19910628

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EFFECTIVE DATE: 20030819
LEG - OPP
Alive
UP - 2003-46

1 / 1 CRXX - ©CLAIMS/RRX
PN - 5,218,561 A 19930608 [US5218561]
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ACT - 20030819 REISSUE REQUESTED
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